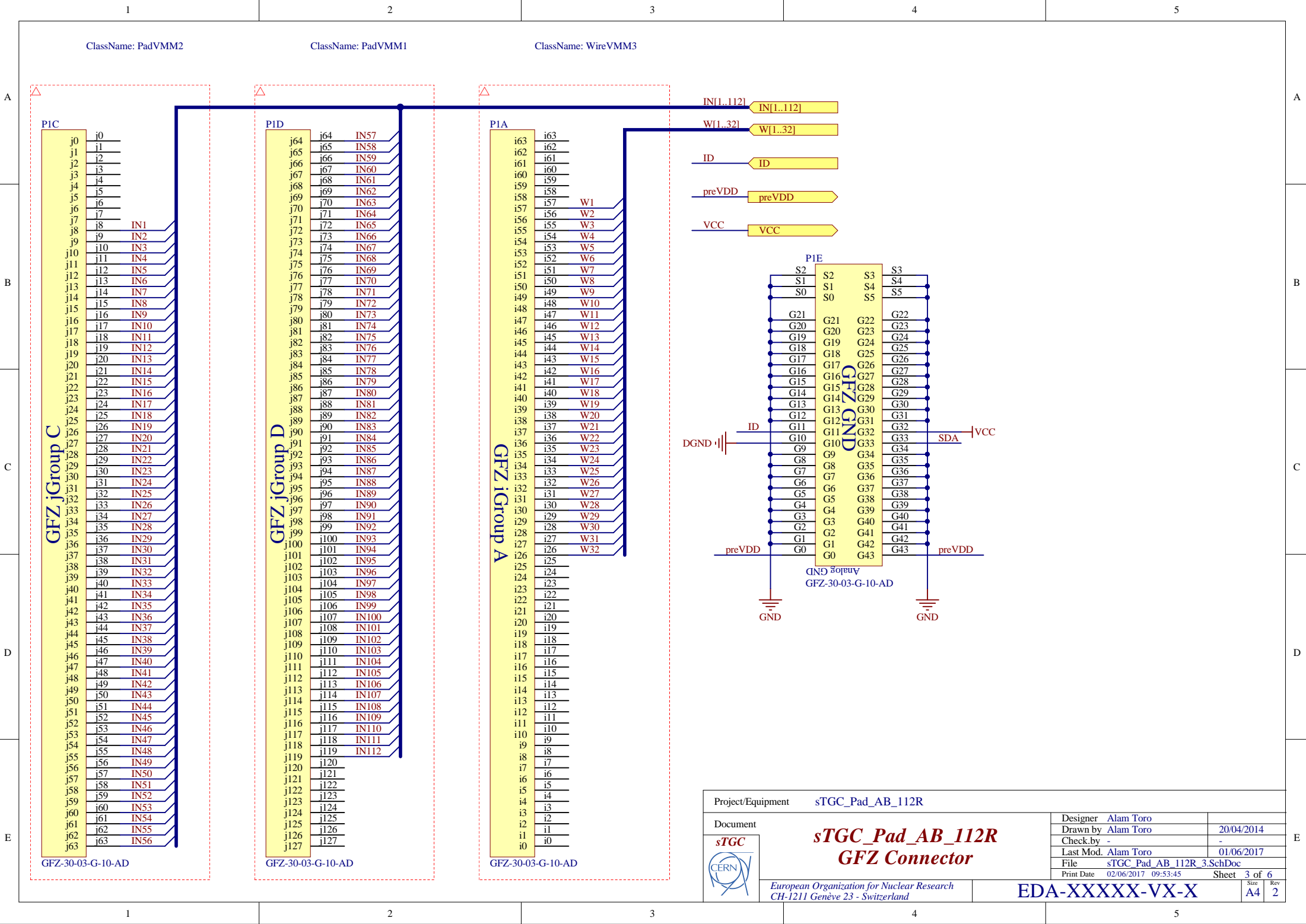
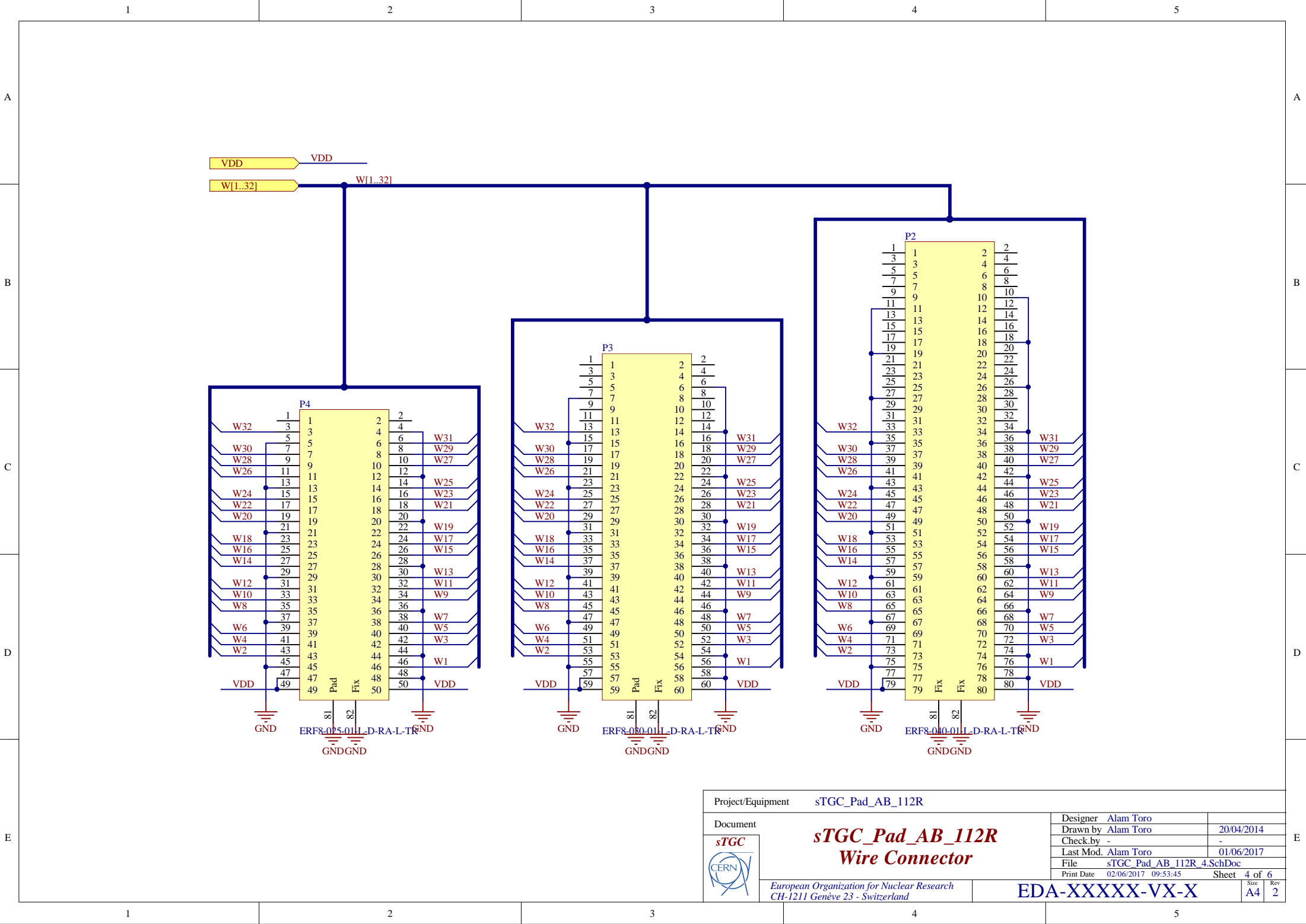



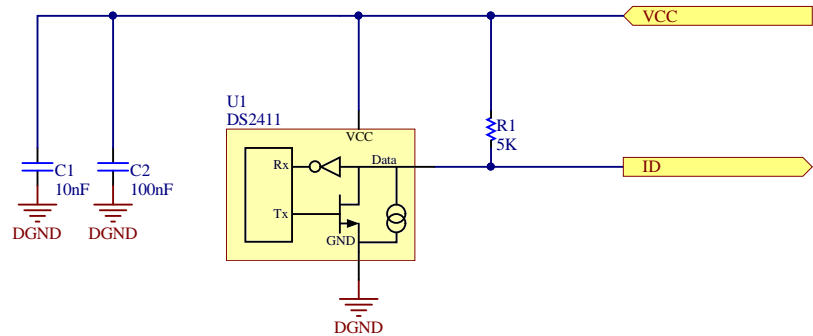
Project/Equipment sTGC_Pad_AB_112R		
<div><div>sTGC</div><div>CERN</div></div>	Document	
	sTGC_Pad_AB_112R Detector Edge	
Designer Alam Toro		
Drawn by Alam Toro		20/04/2014
Check by -		
Last Mod. Alam Toro		01/06/2017
File sTGC_Pad_AB_112R_2.SchDoc		
Print Date 02/06/2017 09:53:44		Sheet 2 of 6
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X
		Size A4
		Rev 2



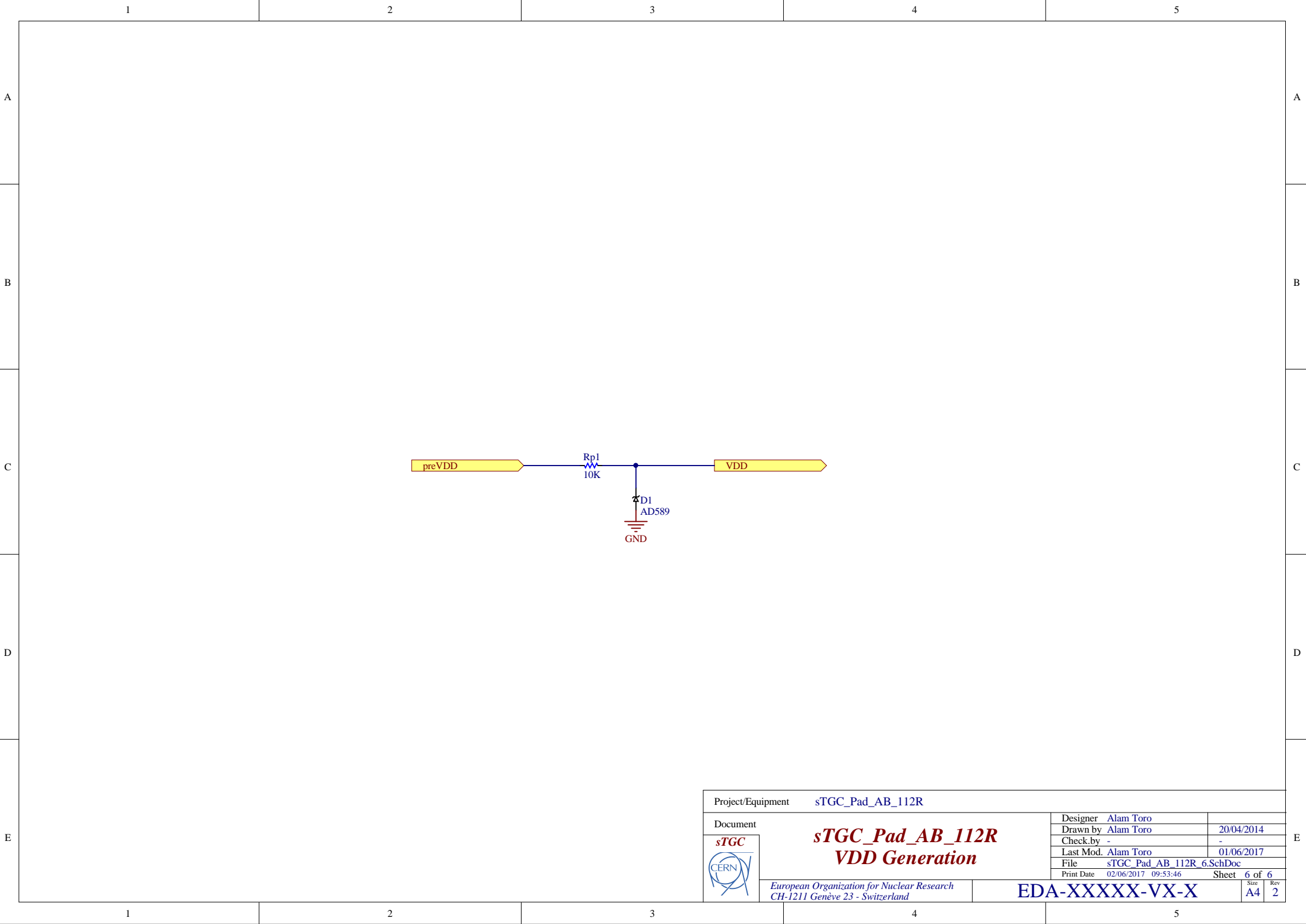
Project/Equipment		sTGC_Pad_AB_112R	
<div><div>sTGC</div><div>CERN</div></div>	Document		<b>sTGC_Pad_AB_112R</b> <b>GFZ Connector</b>
	Designer	Alam Toro	
	Drawn by	Alam Toro	20/04/2014
	Check by	-	-
	Last Mod.	Alam Toro	01/06/2017
File		sTGC_Pad_AB_112R_3.SchDoc	
Print Date		02/06/2017 09:53:45	Sheet 3 of 6
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXXX-VX-X	
		Size	Rev
		A4	2



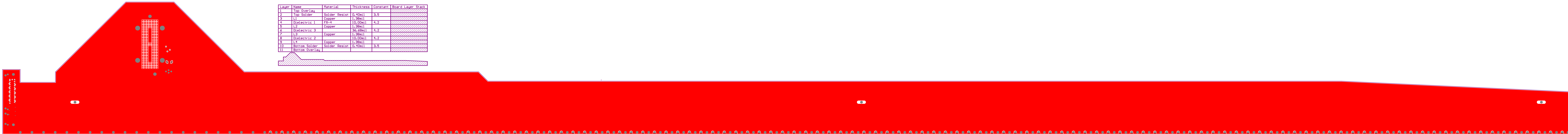
Project/Equipment		sTGC_Pad_AB_112R	
Document		<b>sTGC_Pad_AB_112R</b> <b>Wire Connector</b>	
	Designer	Alam Toro	
	Drawn by	Alam Toro	20/04/2014
	Check by	-	-
	Last Mod.	Alam Toro	01/06/2017
	File	sTGC_Pad_AB_112R_4.SchDoc	
Print Date		02/06/2017 09:53:45	Sheet 4 of 6
European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland		EDA-XXXXX-VX-X	
		Size	Rev
		A4	2



Project/Equipment			sTGC_Pad_AB_112R		
<div><div>sTGC</div><div>CERN</div></div> <div><div>sTGC_Pad_AB_112R</div><div>Identification Chip</div></div> <div>European Organization for Nuclear Research</div> <div>CH-1211 Genève 23 - Switzerland</div>			Designer	Alam Toro	
			Drawn by	Alam Toro	20/04/2014
			Check.by	-	-
			Last Mod.	Alam Toro	01/06/2017
			File	sTGC_Pad_AB_112R_5.SchDoc	
			Print Date	02/06/2017 09:53:46	Sheet 5 of 6
			EDA-XXXXX-VX-X		
			Size	A4	Rev 2

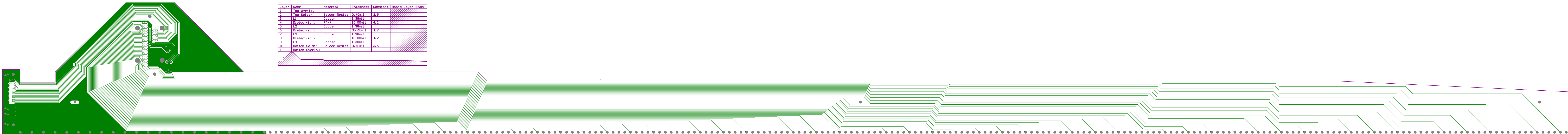


Project/Equipment			sTGC_Pad_AB_112R		
<div><div>sTGC</div><div>CERN</div></div> <div><div>sTGC_Pad_AB_112R</div><div>VDD Generation</div></div> <div>European Organization for Nuclear Research CH-1211 Genève 23 - Switzerland</div>			Designer	Alam Toro	
			Drawn by	Alam Toro	20/04/2014
			Check.by	-	-
			Last Mod.	Alam Toro	01/06/2017
			File	sTGC_Pad_AB_112R_6.SchDoc	
			Print Date	02/06/2017 09:53:46	Sheet 6 of 6
			EDA-XXXXXX-VX-X		
			Size	A4	Rev 2

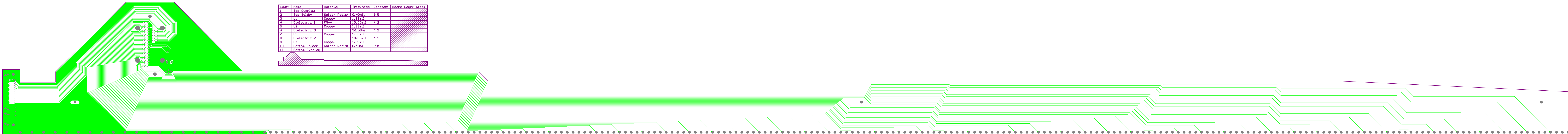


Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	1.38mil		
4	Dielectric 1	FR-4	10.00mil	4.2	
5	L2	Copper	1.38mil		
6	Dielectric 3		36.68mil	4.2	
7	L3	Copper	1.38mil		
8	Dielectric 2		10.00mil	4.2	
9	L4	Copper	1.38mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

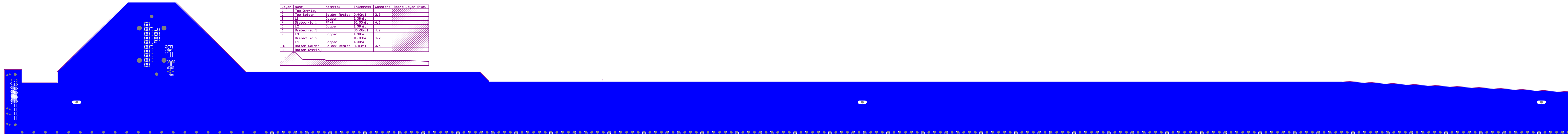




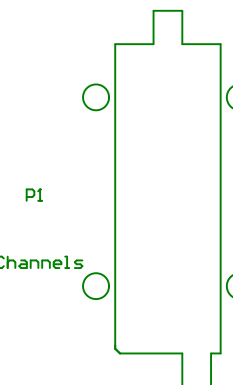




Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	1.38mil		
4	Dielectric 1	FR-4	10.00mil	4.2	
5	L2	Copper	1.38mil		
6	Dielectric 3		36.68mil	4.2	
7	L3	Copper	1.38mil		
8	Dielectric 2		10.00mil	4.2	
9	L4	Copper	1.38mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



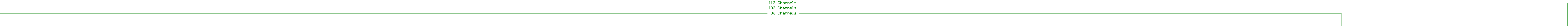
Pad Adapter Board 112 Channels  
sTGC, NSM, ATLAS, CERN  
RIGHT

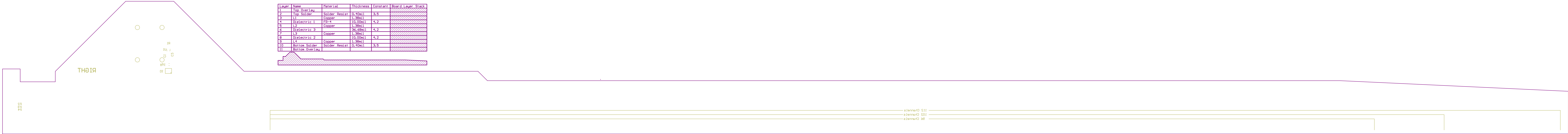


Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				[Hatched Pattern]
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	1.38mil		[Hatched Pattern]
4	Dielectric 1	FR-4	10.00mil	4.2	
5	L2	Copper	1.38mil		[Hatched Pattern]
6	Dielectric 3		36.68mil	4.2	
7	L3	Copper	1.38mil		[Hatched Pattern]
8	Dielectric 2		10.00mil	4.2	
9	L4	Copper	1.38mil		[Hatched Pattern]
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				[Hatched Pattern]



112 Channels  
102 Channels  
96 Channels









Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	1.38mil		
4	Dielectric 1	FR-4	10.00mil	4.2	
5	L2	Copper	1.38mil		
6	Dielectric 3		36.68mil	4.2	
7	L3	Copper	1.38mil		
8	Dielectric 2		10.00mil	4.2	
9	L4	Copper	1.38mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

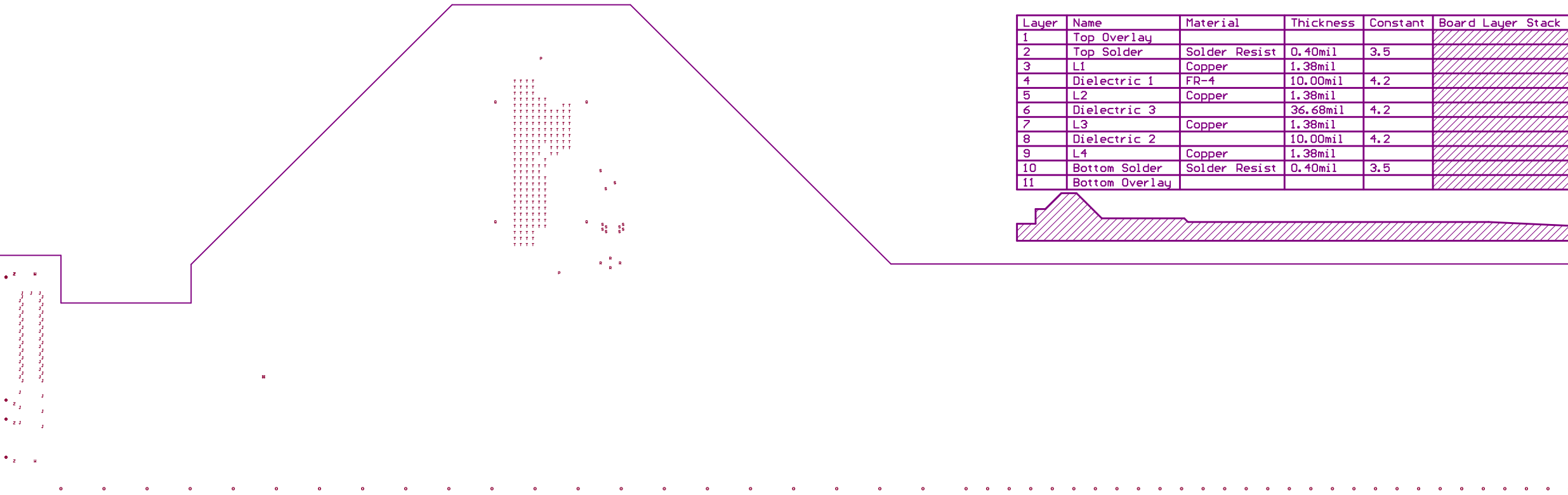


Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	1.38mil		
4	Dielectric 1	FR-4	10.00mil	4.2	
5	L2	Copper	1.38mil		
6	Dielectric 3		36.68mil	4.2	
7	L3	Copper	1.38mil		
8	Dielectric 2		10.00mil	4.2	
9	L4	Copper	1.38mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				









Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	1.38mil		
4	Dielectric 1	FR-4	10.00mil	4.2	
5	L2	Copper	1.38mil		
6	Dielectric 3		36.68mil	4.2	
7	L3	Copper	1.38mil		
8	Dielectric 2		10.00mil	4.2	
9	L4	Copper	1.38mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				



Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length
P	2	1.691mm <65.00mil>	PTH	Round	-
⌀	3	2.000mm <78.74mil>	NPTH	Slot	6.437mm <253.43mil>
R	4	1.000mm <39.37mil>	PTH	Round	-
W	4	1.905mm <75.00mil>	PTH	Round	-
Q	4	2.000mm <78.74mil>	PTH	Round	-
⌀	6	0.635mm <25.00mil>	PTH	Round	-
Z	6	1.448mm <57.00mil>	PTH	Round	-
S	11	0.400mm <15.75mil>	PTH	Round	-
J	55	0.254mm <10.08mil>	PTH	Round	-
T	184	0.254mm <10.08mil>	PTH	Round	-
G	246	1.350mm <53.15mil>	PTH	Round	-
	525 Total				

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.  
Physical Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout





Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	L1	Copper	1.38mil		
4	Dielectric 1	FR-4	10.00mil	4.2	
5	L2	Copper	1.38mil		
6	Dielectric 3		36.68mil	4.2	
7	L3	Copper	1.38mil		
8	Dielectric 2		10.00mil	4.2	
9	L4	Copper	1.38mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				